Roll No.

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B. Tech(IT) (Full Time) - END SEMESTER EXAMINATIONS, NOV/DEC 2024

Information Technology
IV Semester

IT5451 COMPUTER ARCHITECTURE

(Regulation 2019)

Time: 3hrs | Max.Marks: 100

CO 1	Interpret assembly language instructions
CO 2	Design and analyze ALU circuits
CO 3	Implement a control unit as per the functional specification.
CO 4	Design and analyze memory, I/O devices and cache structures for processor
CO 5	Evaluate the performance of computer systems.
CO 6	Point out the hazards present in a pipeline and suggest remedies

BL – Bloom's Taxonomy Levels
(L1 - Remembering, L2 - Understanding, L3 - Applying, L4 - Analysing, L5 - Evaluating, L6 - Creating)

PART- A (10 x 2 = 20 Marks)
(Answer all Questions)

Q. No	Questions	Marks	CO	BL
1	Compare CISC and RISC architecture.	2	CO2	L2
2	State the Amdahl's law.	2	CO4	L2
3	Write the booth's code and bit-pair recoding for the given multiplier. A. $(1111010)_2$	2	CO2	L3
4	Perform 37-23 and 47+26 in binary mode by assuming that the register has 8 bits among which one bit is reserved for the sign..	2	CO2	L3
5	What is Hazard? Is WAR an hazard? Give example.	2	CO6	L1
6	Draw the hardwired control circuit for generating PC_{in}.	2	CO5	L2
7	Define Memory access time. How is it affected by the hit ratio?	2	CO4	L2
8	What is early restart ? how does it affect processor waiting time.	2	CO4	L2
9	What is Dynamic scheduling? Can CPI be reduced by using it?	2	CO5	L1
10	How does GPU devices enable parallel programming?.	2	CO5	L2

PART- B (5 x 13 = 65 Marks)

Q. No	Questions	Marks	CO	BL
11 (a) (i)	Write RISC style program to find the number of Mod 5 numerals in a list of **n** words stored in memory. Let the list be stored in the memory locations starting from MOD and **n** be a 32-bit word stored in address COUNT. Store the count value in memory location FIVE.	9	CO1	L3
(ii)	What is Program Status Word? List four commonly used status	4	CO2	L2

	bits and write their use.			
	OR			
11 (b) (i)	Explain the ISA of MIPS processor. Write a short notes on the different types of addressing modes with an example for each.	**9**	CO1	L1
(ii)	Registers R4 and R5 contains the decimal numbers 5000 and 8000. Identify the addressing modes and write is the effective address for each case of addressing mode. a. 12(R4) b. (R4, R5) c. 22(R4,R5) d. (R4)	**4**	CO1	L2
12 (a) (i)	Explain the block schematic for binary division and perform the division on the following 5-bit unsigned integer using Non restoring division: 01110/011.	**7**	CO2	L3
	Explain the design of an Fast Adder. How is the latency improved as compared to ripple adder. Design and Implement the generate and propagate expression for performing carry look ahead addition for an 4bit Adder circuit.	**6**	CO2	L3
	OR			
12 (b) (i)	Compute the Bit pair recoding multiplication of A and B where A=1010 (Multiplicand) and B=1011 (Multiplier).	**6**	CO2	L3
(ii)	Explain the standard IEEE floating point representation. Compare single and double precision format	**7**	CO2	L3
13 (a) (i)	Explain the different types of hazards in a pipelined processor. Elaborate the true data dependency. Narrate different solutions for it.	**13**	CO6	L4
	OR			
13 (b) (i)	Write the control sequence generated for micro instruction routine for the execution of instruction MOV R2, R3. Write a Boolean expression for MDR_{in} , End and IR_{in} for the hardwired encoder of the control unit.	**13**	CO3	L3
14 (a) (i)	Explain the different cache mapping techniques. How are page replacement policies affected by them.	**13**	CO4	L3
	OR			
14 (b) (i)	What is Virtual memory? Justify the need for it. Explain the Virtual memory address is translation in to physical address and write how TLB improve the performance of Virtual memory	**13**	CO4	L1
15 (a) (i)	Explain Tomasulo's algorithm. Compare it with scoreboard technique.	**13**	CO5	L3
	OR			
15 (b) (i)	Explain the evolution of GPU processor. Compare it with vector based processor architecture.	**13**	CO5	L5

PART- C (1 x 15 = 15 Marks)

(Q.No.16 is compulsory)

Q. No	Questions	Marks	CO	BL
16. (i)	Design an ALU for a RISC processor with two logical and two arithmetic instruction. Decide the addressing mode. Consider the dual Datapath internal bus organization. Consider the processor is specific for Geo Spatial application. How do you improve it for enhancing SIMD programs	**15**	CO5	L3